Siyuan Chen

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Research Interests

I'm a computer architect and a chip-building VLSI engineer with sub-28nm tapeout experiences. My research interests are in agile hardware design and the design of flexible accelerators for applications like deep learning and robotics.

Education

Carnegie Mellon University, Pittsburgh, PA August 2020 – December 2025
Expected Ph.D. in Electrical and Computer Engineering
Advisor: Dr. Ken Mai
Cumulative GPA: 4.00/4.00

Carnegie Mellon University, Pittsburgh, PA August 2020 – May 2022
M.S. in Electrical and Computer Engineering
Advisor: Dr. Ken Mai
Cumulative GPA: 4.00/4.00

Duke University, Durham, NC August 2017 – May 2020
B.S.E. Electrical and Computer Engineering, 2nd Major in Computer Science
Advisor: Dr. Krishnendu Chakrabarty
Cumulative GPA: 3.887/4.000

Research Experience

Academia

Research Assistant, Carnegie Mellon University, Pittsburgh, PA October 2020 - Present

Flexible and Low-Bandwidth Sparse Neural Network Accelerator in 22nm **[ESSERC'24]**

- Designed a sparse neural network accelerator that achieves high hardware utilization across different types of layers with an improved channel-last dataflow
- Test chip in Intel 22nm FinFET achieves 9.52TOPs/W (114MHz at 0.55V) when running a sparse ResNet-18
- Reduced the off-chip data communication bandwidth by 11.8x with a new model-level dataflow

Towards Specialized Hardware for Learning-based Visual Odometry **[IROS'22]**

- Proposed a heterogeneous System-on-Chip architecture to accelerate deep-learning-based visual odometry on energy-constrained robots
- Redesigned three state-of-the-art algorithms based on characteristics of the proposed hardware using pruning, quantization and parameter tuning to improve their energy efficiency
- Implemented all algorithms on Xilinx FPGAs using the Xilinx Deep-learning Processing Unit IP with an improved energy efficiency of 2.7x compared to NVIDIA's Jetson Nano embedded computer

High-Performance FFT Accelerator in 28nm **[HPEC'22, HotChips'24]**

- Implemented the physical design of a Fast Fourier Transform (FFT) hardware accelerator in TSMC 28nm
- Achieved 1GHz in silicon and 86x improvement on energy-delay product compared to a similar academic FFT accelerator design by fully unrolling and deeply pipelining our proposed accelerator

Research Assistant, Duke University, Durham, NC August 2018 – July 2020

Detection of Rowhammer Attacks in FPGA-SoCs **[TCAD'21, ETS'20]**

- Developed a hardware monitor that listens to FPGA-SDRAM memory transactions to detect Rowhammer attacks in heterogeneous FPGA System-on-Chips
- Verified resilience of solution against different variants of Rowhammer attacks on real hardware while consuming only 1% of FPGA resources

Industry

Platform Architecture Intern, Apple Inc., Cupertino, CA Summer 2023, 2024
Supervisor: Dr. Jaewon Shin
- Performed architectural workload analysis on Apple Neural Engine

Research Intern, IBM Research, Yorktown Heights, NY Summer 2019
Supervisor: Dr. Gi-Joon Nam
BISTLock, Efficient Logic Locking with BIST **[ITC'21, ITC'20]**
- Proposed a protection method against semiconductor IP piracy that locks an IC in test mode until a correct key is provided to the build-in self-test (BIST) module

Teaching Assistant

CMU	18-622	Digital Integrated Circuits Design	Fall 2023
CMU	18-726	Projects in Integrated Circuit Design: First Silicon	Fall 2022, 2023
CMU	18-725	Advanced Digital Integrated Circuit Design	Spring 2022, 2024
Duke	ECE 550	Fundamentals of Computer Systems and Engineering	Fall 2019
Duke	ECE 350	Digital Systems	Spring 2019, Fall 2019, Spring 2020

Publications

Journal Papers

[1] Rana Elnaggar, **Siyuan Chen**, Peilin Song, Krishnendu Chakrabarty, "Securing SoCs with FPGAs Against Rowhammer Attacks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, August 2021.
[2] Yuanyong Luo, Yuxuan Wang, Yajun Ha, Zhongfeng Wang, **Siyuan Chen** and Hongbing Pan, "Generalized Hyperbolic CORDIC and Its Logarithmic and Exponential Computation With Arbitrary Fixed Base", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (**TVLSI**)*, September 2019.

Conference Papers

[1] **Siyuan Chen** and Ken Mai, "A 22nm 9.52TOPs/W Sparse Neural Network Accelerator with Grouped Hierarchical Accumulation for Edge Perception", *IEEE European Solid-State Electronics Research Conference (**ESSERC**)*, 2024.
[2] Larry Tang, **Siyuan Chen**, Keshav Harisrikanth, Guanglin Xu, Franz Franchetti and Ken Mai, "A 1.19GHz 9.52 Gsamples/sec Radix-8 FFT Hardware Accelerator in 28nm", *IEEE Hot Chips Symposium (**HotChips**)*, 2024.
[3] **Siyuan Chen** and Ken Mai, "Towards Specialized Hardware for Learning-based Visual Odometry on the Edge", *IEEE/RSJ International Conference on Intelligent Robots and Systems (**IROS**)*, 2022.
[4] Larry Tang, **Siyuan Chen**, Keshav Harisrikanth, Guanglin Xu, Ken Mai and Franz Franchetti, "A High Throughput Hardware Accelerator for FFTW Codelets: A First Look", *IEEE High Performance Extreme Computing (**HPEC**)*, 2022.
[5] Jonti Talukdar, **Siyuan Chen**, Amitabh Das, Sohrab Aftabjahani, Peilin Song and Krishnendu Chakrabarty, "A BIST-based Dynamic Obfuscation Scheme for Resilience against Removal and Oracle-guided Attacks", *IEEE International Test Conference (**ITC**)*, October 2021.
[6] **Siyuan Chen**, Jinwook Jung, Peilin Song, Krishnendu Chakrabarty and Gi-Joon Nam, "BISTLock: Efficient IP Piracy Protection using BIST", *IEEE International Test Conference (**ITC**)*, November 2020.
[7] Rana Elnaggar, **Siyuan Chen**, Peilin Song, Krishnendu Chakrabarty, "Detection of Rowhammer Attacks in SoCs with FPGAs", *IEEE European Test Symposium (**ETS**)*, May 2020.

Awards

Apple Ph.D Fellowship	Apple	2023, 2024
Dean's Fellowship	CMU	2020
Charles Ernest Seager Memorial Award	Duke	2020

(recognizes outstanding undergraduate research)

Technical Skills

Hardware/Programming Languages: Verilog, Chisel, Python, Tcl, C, Java, MATLAB
EDA Tools: Cadence {Genus, Innovus, Voltus, Virtuoso, Liberate, NCSim}, Mentor Calibre, Xilinx Vivado